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AN IMPROVED SEA BOTTOM CLASSIFIER

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PANAMA CITY, FLORIDA 32401

NAVAL COASTAL SYSTEMS LABORATORY

ABSTRACT

An improved Sea Bottom Classifier device configured for use with a towed underwater vehicle is described. Operating on the same basic principles as earlier models, but including several refinements, the device provides a relative indication of sea bottom hardness. Some preliminary sea test results are given along with a detailed discussion of the circuits of the improved device.

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GENERAL SYSTEM DESCRIPTION

The Sea Bottom Classifier (SBC) as configured for use with a towed underwater vehicle consists of five main functional sections: (a) a pulse-type echo ranging sonar for determining the height of the towed vehicle above the sea bottom and to provide an echo signal for sea bottom type analysis, (b) signal processing circuitry for sea bottom type analysis, (c) an interface circuit between the SBC echo ranging sonar and the towed vehicle bottom contour-following servo system, (d) a power supply to provide proper operating voltages to the SBC circuits, and (e) a paper chart recorder for display and recording of sea bottom type information. The echo ranging circuits in the towed vehicle that normally provide the bottom contour-following servo system with vehicle altitude information are disabled because this information is provided by the SBC. A block diagram of the system is shown in Figure 1.

The SBC described herein operates on the same basic principle as earlier models.[1] That is, the sea bottom type is determined from an analysis of the bottom-echo signal for pulse time duration increase due to sound penetration into the sea bottom. This is done by measuring the time duration of the bottom-echo-signal envelope between the beginning of the pulse and the point where the envelope level is approximately 37 percent of its peak value. The time duration of the transmitted pulse is subtracted from the bottom-echo pulse-time duration and the difference is the increase in time duration of the bottom-echo pulse due to penetration. This increase is averaged over many bottom echoes and displayed as sea bottom type ranging from hard for shell and sand bottoms to soft for mud bottoms. The SBC described herein differs from earlier models in several important respects:

1. A self-contained echo-ranging sonar allows independent operation of the SBC by providing its own signal for analysis.

2. Wide-range automatic gain control in the SBC receiver allows operation over all bottom types without manual gain adjustment.

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[1] Mine Defense Laboratory Report N2739, *Acoustic Sea Bottom Classifier*, by W. C. Stanley and G. W. Harris, July 1968 (Unclassified).

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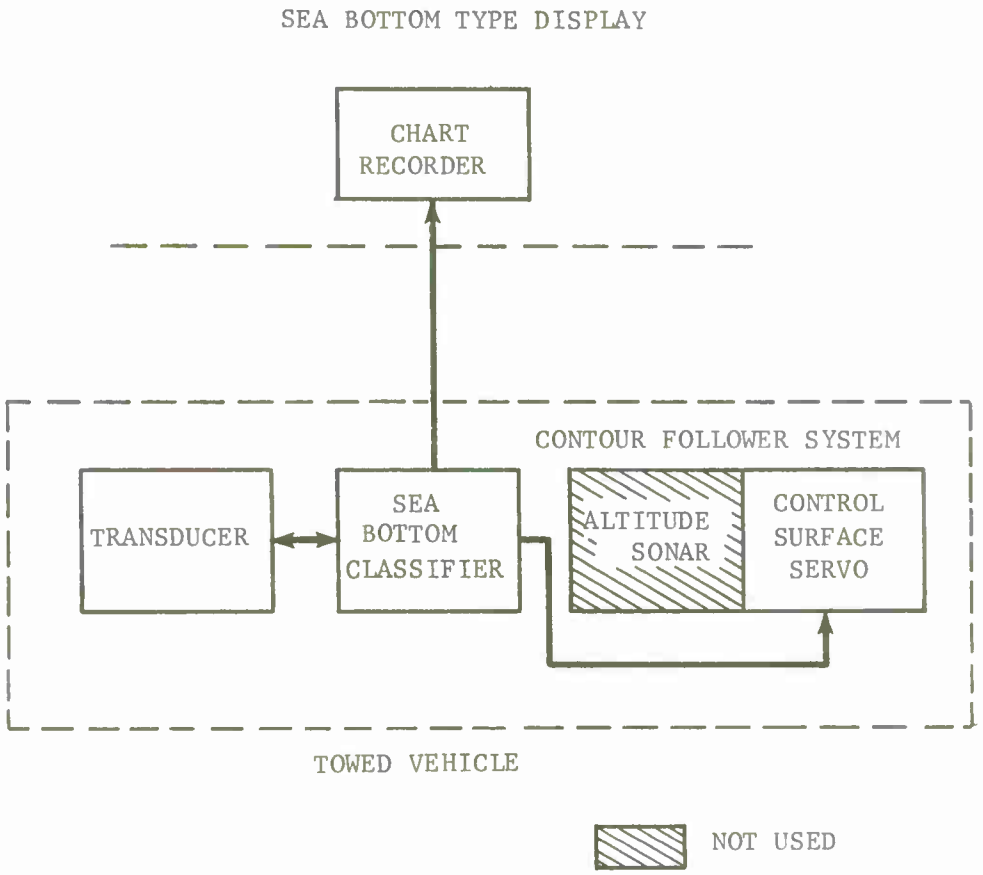

FIGURE 1. SYSTEM BLOCK DIAGRAM

3. Logic circuitry allows only the first bottom-echo signal to be processed, thereby eliminating erroneous readings due to multipath.

4. The use of an automatic compensation circuit reduces the error in bottom type readout caused by vehicle altitude changes.

5. The use of linear and digital integrated circuits allows more circuit sophistication in a comparable physical size while providing more reliable operation under conditions of varying temperature.

6. The use of a paper chart recorder provides simultaneous display and permanent storage of sea bottom type information.

PRELIMINARY SEA TEST RESULTS

Preliminary sea tests of the SBC were conducted at selected sites in the Gulf of Mexico and St. Andrew Bay, Panama City, Florida. The locations of the various sites are shown in Figure 2.

In addition to taking SBC bottom hardness readings, gravity penetrometer tests were conducted by divers at the various sites. The SBC bottom hardness readings with a range of 0 to 1.0 are compared with the results of the penetrometer tests in Table 1.

TABLE 1

COMPARISON OF SBC AND PENETROMETER READINGS

Site	Mean SBC Reading (volts)	Penetrometer Penetration (cm)
1. Gulf of Mexico	0.10	2.0
2. Courtney Point	0.27	26.6
3. Shipyard	0.30	25.4
4. St. Andrew Bay	0.35	47.0
5. Turn Buoy	0.55	53.2
6. Near Gulf Coast College	0.80	68.4

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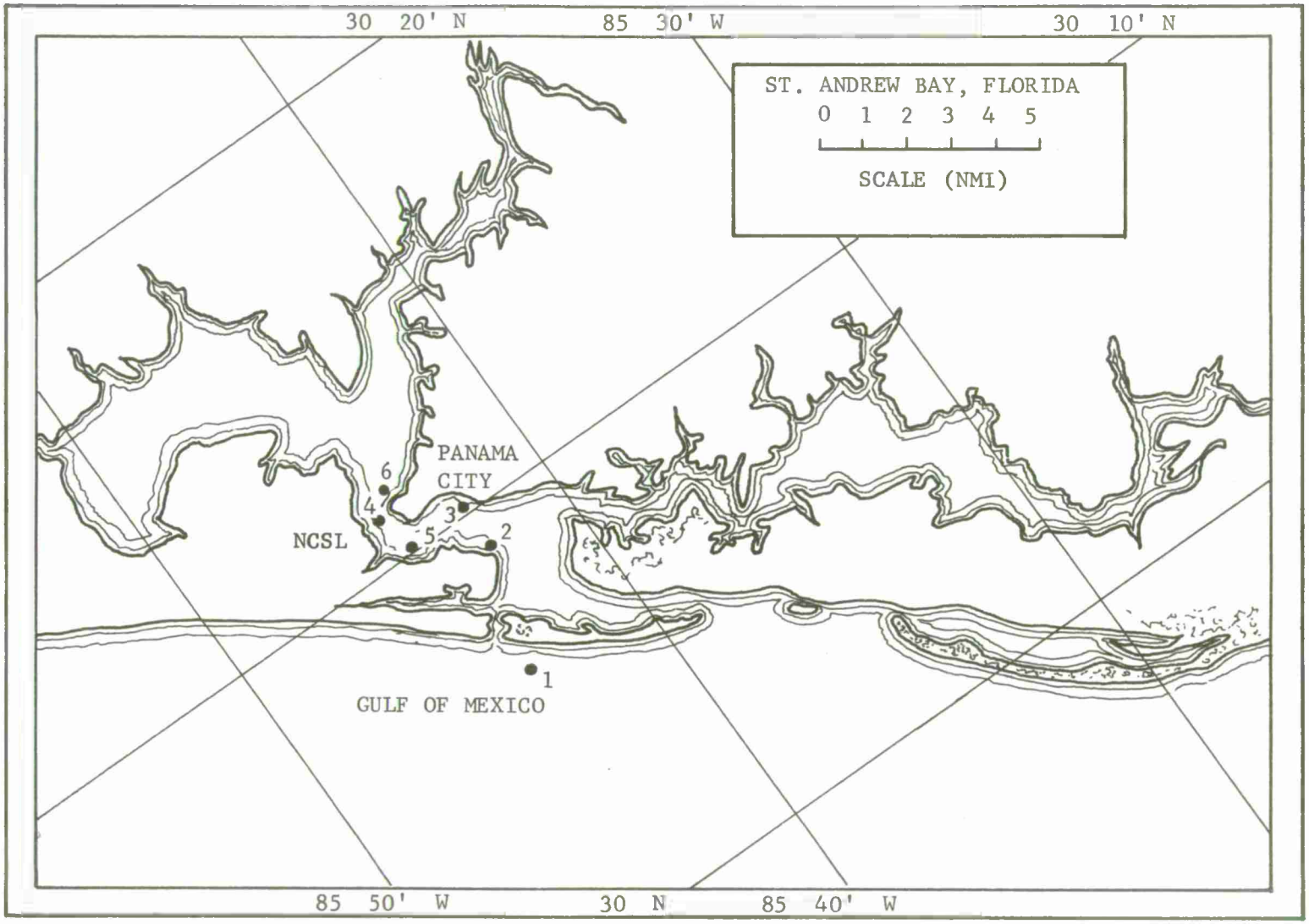

FIGURE 2. SBC TEST SITES

The results shown in Table 1 represent the analysis of a relatively small amount of data. While sufficient to show that the SBC is operating as expected, the amount of data is insufficient to accurately correlate the SBC bottom type reading with the depth of penetrometer penetration. The collection and analysis of sufficient data should provide this correlation. Since the relationship between bottom shear strength and depth of penetrometer penetration is known, the SBC chart recorder could be calibrated in bottom shear strength units.

Typical SBC chart recordings are shown in Figure 3. The chart recorder speed was one division per 5 seconds and the towed vehicle speed was approximately 1.5 meters per second, giving a horizontal distance scale of approximately 7.5 meters per division. The vertical scale is 0.1 volt per major division. Figure 3A shows the SBC response to the hard sand bottom at site 1 in the Gulf of Mexico. Figure 3B shows the SBC response to the mud bottom at site 6 near Gulf Coast College. The sudden rise in the chart trace between two and three divisions from the left end of the chart was caused by a school of fish swimming just above the bottom. Figure 3C is the SBC response at site 6 with the towed vehicle path slightly different from that in Figure 3B.

There are three sources of error in the SBC bottom analysis that have been observed. The SBC analyzes the first received echo and ignores any others. Therefore, it will analyze the echo from a school of fish above the bottom and ignore the bottom. This is a transient error and should not be significant. The SBC may give an erroneous indication when operating over a very irregular bottom, such as sand with outcroppings of rock, due to multipath phenomena. However, the sonar operator would be aware of the presence of such a bottom from sonar data. The third source of error is a change in vehicle altitude (that is, a change in distance between the bottom and the SBC transducer). As the altitude increases, the apparent echo-pulse duration increases indicating a softer bottom. This error has been reduced by internal compensation which should prove to be entirely adequate but is awaiting further tests and evaluation.

CIRCUIT BOARD FUNCTIONS

The SBC consists of five etched circuit boards with individual functions as shown in Figure 4. Basic circuit board functions will be discussed after which individual circuits will be covered in detail.

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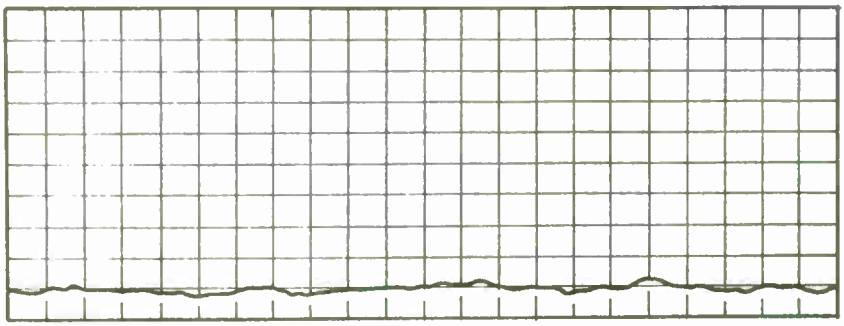
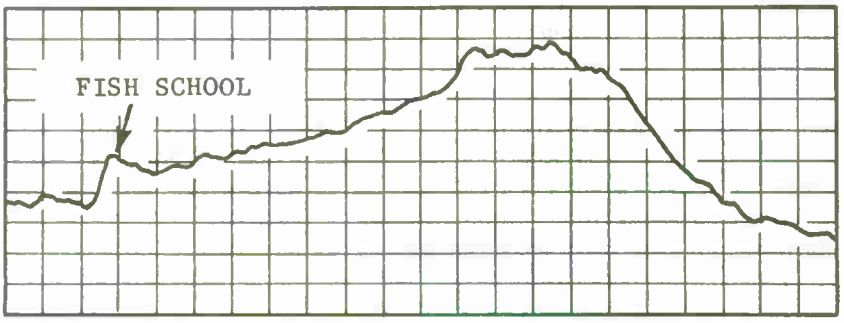
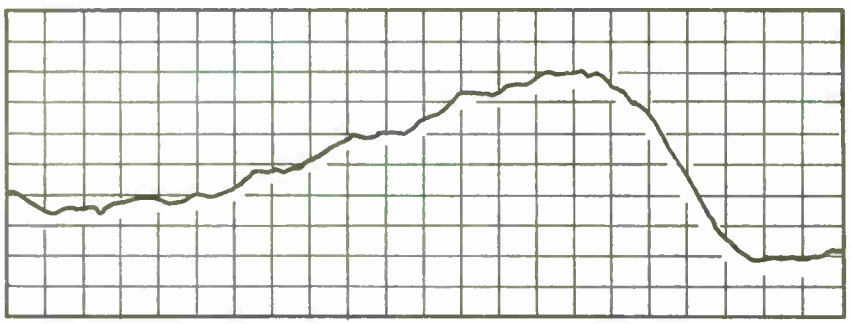


A. GULF SITE 1 SAND BOTTOM



B. NEAR GULF COAST COLLEGE SITE 6 MUD BOTTOM



C. NEAR GULF COAST COLLEGE SITE 6 MUD BOTTOM

HORIZONTAL SCALE APPROXIMATELY
7.5 METERS PER DIVISION

FIGURE 3. TYPICAL SBC CHART RECORDINGS

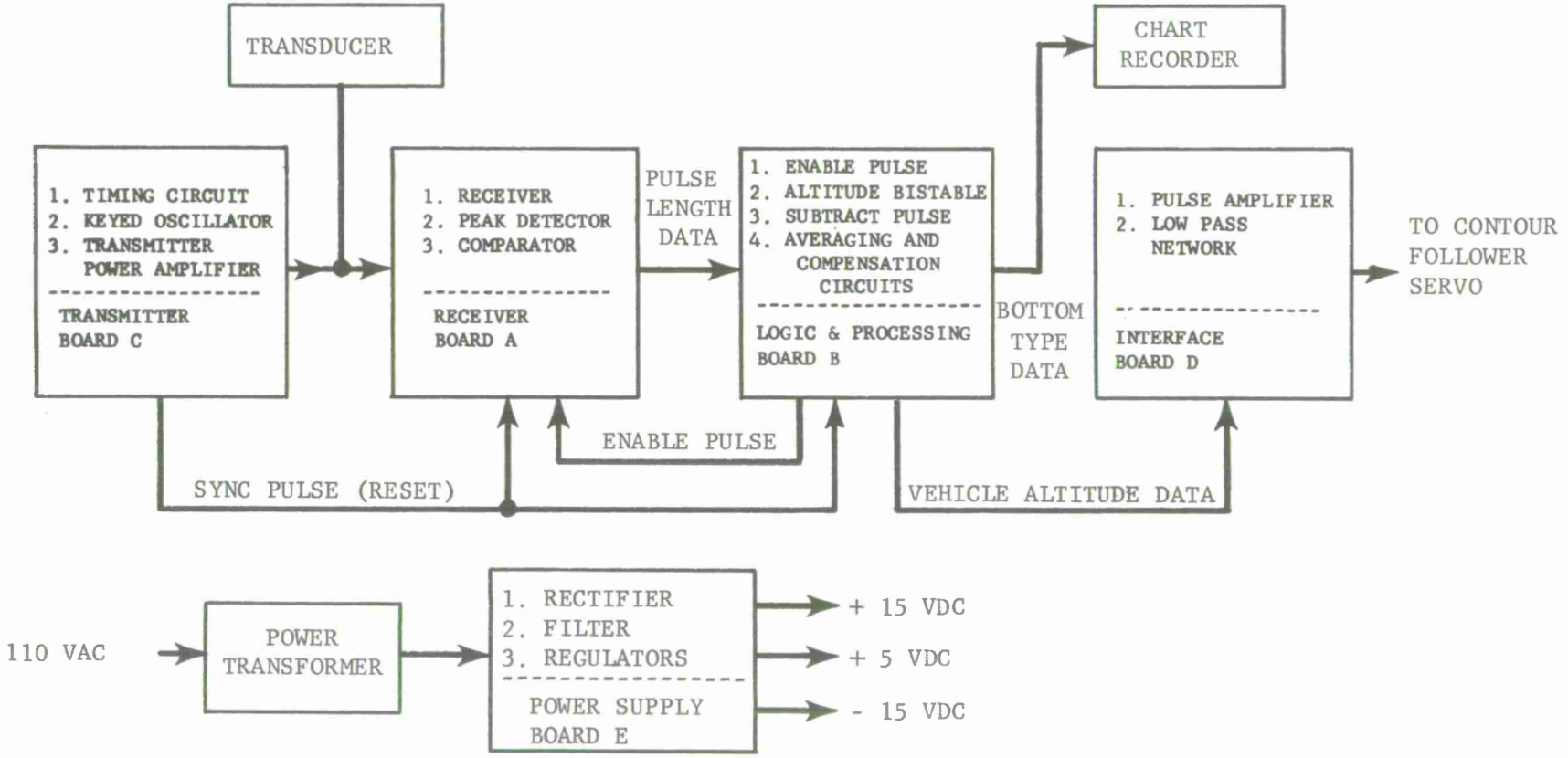


FIGURE 4. SBC BLOCK DIAGRAM SHOWING CIRCUIT BOARD FUNCTIONS

Circuit board letter designations are based on the physical arrangement of the boards in the system rather than the order of discussion.

The transmitter, board C, generates a pulsed 110 kilohertz signal which drives the transducer. The pulse duration and repetition rate are 1.0 millisecond and 40 pulses per second, respectively. A synchronization pulse is generated which is coincident in time with the beginning of the transmitted pulse.

The receiver, board A, receives the echo signals from the transducer, and amplifies and envelope detects them. The envelope-detected signals are allowed to pass the processing circuits only at the proper time by the enable pulse. This results in only the first bottom-echo signal being processed. The initial signal processing circuits on the receiver board generate a digital output pulse with a time duration equal to the time duration of the bottom-echo signal as defined above.

The logic and processing circuits, board B, generate the enable pulse, vehicle altitude signal, and process the receiver output pulse and vehicle altitude signal to provide compensated bottom type information. The enable pulse activates the processing circuitry at the end of a fixed time delay initiated by the synchronization pulse. This prevents processing of the transmitter signal and close-range volume reverberation for bottom type and AGC information. The enable pulse keeps the processing circuitry activated until the end of a fixed-time delay initiated by the first echo signal received after which time no enable pulse can be generated until the system is reset by the next synchronization pulse. This allows only the first echo pulse to be processed. The vehicle altitude signal is generated by a bistable multivibrator which is set by the synchronization pulse and reset by the bottom-echo signal. Its output signal is a digital pulse with a time duration directly proportional to the vehicle altitude. The processing circuitry on board B generates a reference pulse with a time duration slightly larger than that of the transmitted pulse, and subtracts the reference pulse from the receiver voltage comparator output pulse to provide the bottom type difference pulse. The vehicle altitude signal pulse is clamped to ground and clipped at a negative reference level. This reference pulse is then attenuated and added to the bottom type difference pulse. The composite pulse signal is then averaged by an RC low-pass network and the resultant dc analog signal is amplified and displayed on the chart recorder as sea bottom type information.

The interface circuit, board D, amplifies and averages the vehicle altitude signal from board B thereby producing an analog dc voltage which is compatible with the towed-vehicle contour-follower servo system.

The power supply, board E, rectifies, filters, and regulates the ac voltage from the power transformer to provide the proper dc operating voltages for the system.

CONCLUSIONS

The results of preliminary sea tests of the SBC compared with diver tests and observations indicate that the SBC will indicate the relative hardness of the sea bottom. Further testing and evaluation of the SBC will allow correlation of SBC bottom type readings with sea bottom shear strength.

The SBC described herein is configured for use with a towed underwater vehicle. The SBC is self-contained and will operate independently of the systems.

APPENDIX A

CIRCUITS DESCRIPTION

TRANSMITTER, BOARD C

The schematic circuit diagram of the transmitter, board C, is shown in Figure A1. Complementary unijunction transistor Q_1 operates as a conventional relaxation oscillator adjusted to produce a trigger pulse every 25 milliseconds. Transistor Q_2 is a conventional emitter follower driving the level sensitive input of IC_1, a TTL integrated circuit monostable multivibrator. IC_1 generates a pair of complementary output pulses of 1.0 millisecond duration. The logical 1 output pulse serves as the system synchronization pulse while the logical 0 output pulse keys the transmitter oscillator, consisting of transistors Q_3, Q_4, and associated circuitry. Transistor Q_4 is basically a Q-multiplier circuit with sufficient positive feedback for oscillation. When transistor Q_3 is turned on, a dc current flows through L_1, CR_3, R_{12}, and saturated transistor Q_3. This shunting of L_1 lowers its Q sufficiently to prevent oscillation. When transistor Q_3 is turned off by a keying pulse from IC_1, diode CR_3 is reverse biased. The magnetic field of L_1 produced by the dc current collapses causing a rapid buildup of oscillations at approximately 110 kilohertz in the tuned circuit. Positive feedback through R_{14} and R_{15} is adjusted to maintain constant amplitude oscillations for the duration of the keying pulse. Transistor Q_5 is a conventional emitter follower for buffering the oscillator output. Transistor Q_6 operates as a paraphase amplifier to provide a push-pull drive signal for the transmitter power amplifier. Transistors Q_7 and Q_8 are conventional emitter followers for buffering the output of the paraphase amplifier. Transistors Q_9, Q_{10}, Q_{11}, and Q_{12} comprise a class B push-pull power amplifier using a compound connection of transistors to form each half of the push-pull circuit. A small forward bias is provided by resistor dividers R_{27} - R_{28} and R_{29} - R_{30} to reduce crossover distortion. The power amplifier is transformer coupled to the transducer. Inductor L_2 serves to cancel the reactive component of the load impedance due to static capacitance of the transducer and the transducer cable capacitance.

RECEIVER, BOARD A

The receiver board schematic circuit diagram is shown in Figure A2. The input network consisting of R_1, CR_1, and CR_2 is a bipolar clipper circuit used to prevent damage to the preamplifier by the transmitted pulse. Transistors Q_1 and Q_2 comprise a low-noise preamplifier with a voltage gain of approximately 20 decibels. The output of the preamplifier drives IC_1, a Motorola type MC1590G AGC wideband amplifier used

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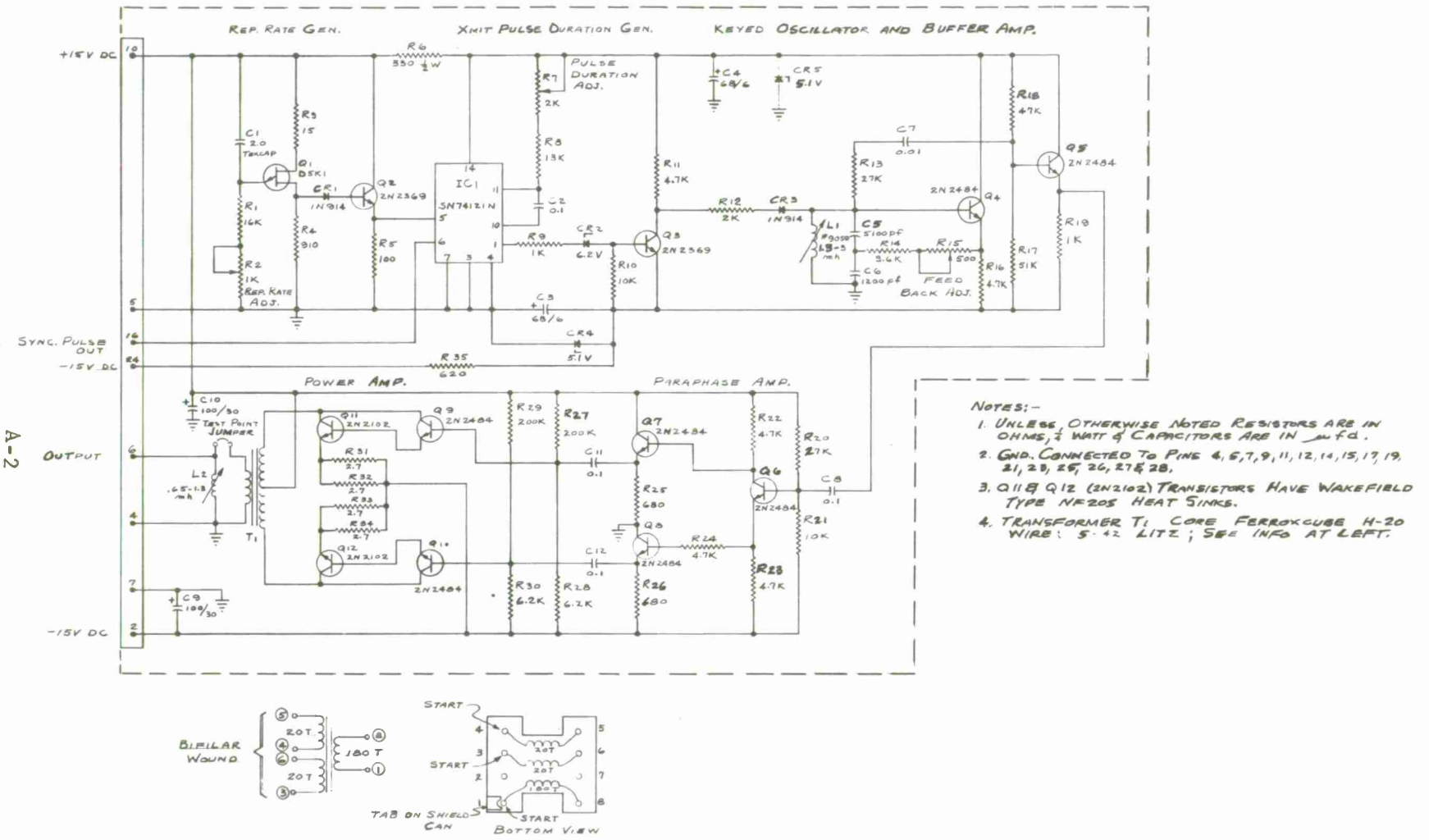
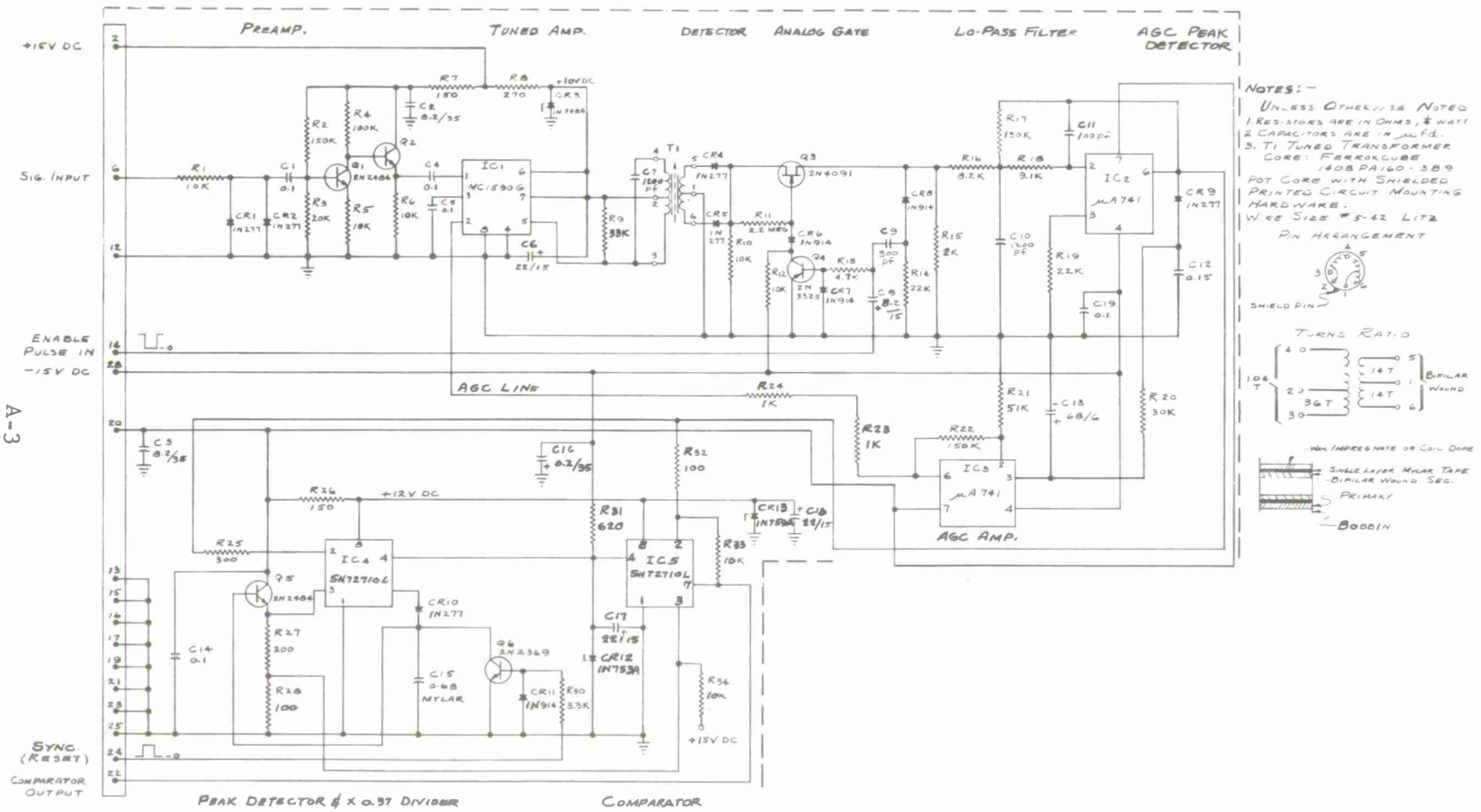


FIGURE A1. SBC TRANSMITTER BOARD C SCHEMATIC



A-3

FIGURE A2. SBC RECEIVER BOARD A SCHEMATIC

with a tuned-transformer collector load which determines the bandwidth of the receiver. The 3-decibel bandwidth of the receiver is approximately 2 kilohertz at a center frequency of approximately 110 kilohertz. The amplified signal from IC_1 is coupled by the tuned transformer to a conventional full-wave rectifier circuit. The rectified signal is coupled to an active low-pass filter through an analog signal gate. Field effect transistor Q_3 and its driver transistor Q_4 constitute the analog signal gate which is turned on by the enable pulse from the logic circuits board B. Capacitor C_9, diode CR_8, and resistor R_{14} serve to couple a portion of the switching signal into the output of the gate in such a manner as to cancel switching transients generated in transistor Q_3 due to its internal capacitance. After passing through the analog signal gate, the signal is applied to IC_2, an internally-compensated integrated-circuit operational amplifier which, with its associated RC network, forms a two-pole active low-pass filter with a nominal passband voltage gain of 20 decibels, a nominal 3-decibel bandwidth of 6 kilohertz, and a nominal high frequency roll-off of 10 decibels per octave. The low-pass filter serves to attenuate the carrier component of the rectified signal and to amplify the resultant envelope-detected signal. The envelope-detected signal is applied to a simple diode-capacitor peak detector CR_9 and C_{12}. The output of this AGC peak detector is filtered by low-pass network R_{20} and C_{13}. The use of a peak detector type AGC makes the AGC voltage less dependent on received-echo-pulse-time duration, thus maintaining a more constant level output pulse from the receiver. The filtered AGC voltage from the low pass network is amplified by IC_3, an internally-compensated integrated-circuit operational amplifier. The amplified AGC voltage is applied to the gain control input of the tuned amplifier IC_1.

The envelope-detected signal is also applied to the peak detector circuit and the voltage comparator circuit both of which utilize type SN72710L integrated circuit voltage comparators. The capacitor C_{15} is charged to the peak voltage of the signal and maintains this voltage until discharged by transistor Q_6 during the synchronization pulse. The transistor Q_5 is an emitter follower used to buffer the storage capacitor to prevent discharge due to the loading effect of the inputs of IC_4 and IC_5. The peak voltage output is taken from emitter follower transistor Q_5 by way of a resistive voltage divider adjusted to deliver an output voltage which is approximately 37 percent of the actual peak value of the detected signal envelope. The envelope-detected signal is connected to the signal input of voltage comparator IC_5 while the 37 percent of peak voltage is connected to the reference voltage input. The voltage comparator output goes to its positive level at the beginning of the received-echo pulse. This level is maintained until the envelope voltage level decays to the 37 percent of peak level maintained by the peak detector at which time the voltage-comparator-output level returns to its negative voltage level.

LOGIC AND PROCESSING, BOARD B

The schematic circuit diagram of the logic circuits, board B, is shown in Figure A3, while the logic timing diagram is shown in Figure A4. The synchronization pulse from the transmitter, board C, is inverted by NAND gate IC_{1a}. The leading edge of the inverted synchronization pulse triggers monostable multivibration IC_2 which generates a positive-going output pulse of approximately 2.8 milliseconds duration as shown in Figure A4b. This time duration determines the time between the transmitted pulse and activation of the processing circuits by the enable pulse. When the output pulse of IC_2 reverts to the logical 0 state, the output of inverter IC_{5b} goes to the logical 1 state (Figure A4c) since both inputs to NOR gate IC_{5a} are logical 0, the output of bistable multivibrator IC_4 having been set to logical 0 by the inverted synchronization pulse (Figure A4d). The logical 1 level at the output of IC_{5b} opens the receiver analog signal gate thus allowing received echo signals to be processed. The output pulse of the receiver voltage comparator (Figure A4e) is inverted by NAND gate IC_{1b}. The inverted-voltage-comparator pulse triggers monostable multivibrator IC_3 which generates a positive-going output pulse of approximately 3 milliseconds duration (Figure A4f). When this output pulse reverts to the logical 0 state it resets the output pulse of bistable multivibration IC_4 to the logical 1 state thus ending the enable pulse.

The inverted synchronization pulse is also applied to the input of the bistable latch circuit consisting of cross-coupled NAND gates IC_{1c} and IC_{1d}. The inverted voltage comparator pulse is applied to the reset input of the bistable latch. The output of the bistable latch, which is the vehicle altitude signal, is therefore a positive-going pulse which is initiated by the synchronization pulse and terminated by the first bottom-echo pulse (Figure A4g). The inverted voltage-comparator pulse is also applied to the trigger input of monostable multivibrator IC_6 and to one input of NOR gate IC_{5d}. The output pulse of monostable multivibrator IC_6, which has a time duration equal to that of the transmitted pulse, is applied to the other input of NOR gate IC_{5d} (Figure A4h). Therefore, the output of NOR gate IC_{5d} is a positive-going pulse with a time duration equal to the difference in time durations of the bottom-echo pulse and the transmitted pulse as shown in Figure A4i. The bistable multivibrator IC_7 disables monostable multivibrator IC_6 after the first output pulse thus allowing only one pulse subtraction per bottom echo pulse. The output of the NOR gate IC_{5d} is buffered by emitter follower transistor Q_1. The inverted vehicle-altitude signal pulse is taken from the output of IC_{1d} and the most positive level is clamped to ground by capacitor C_4 and diode CR_2. Transistor Q_2 is an emitter follower used to buffer the clamp circuit. The negative-going pulse at the output of transistor Q_2 is clipped at minus 2.2 volts by CR_1 as shown in Figure A4j. This negative compensation pulse is

(Text Continued on Page A-8)

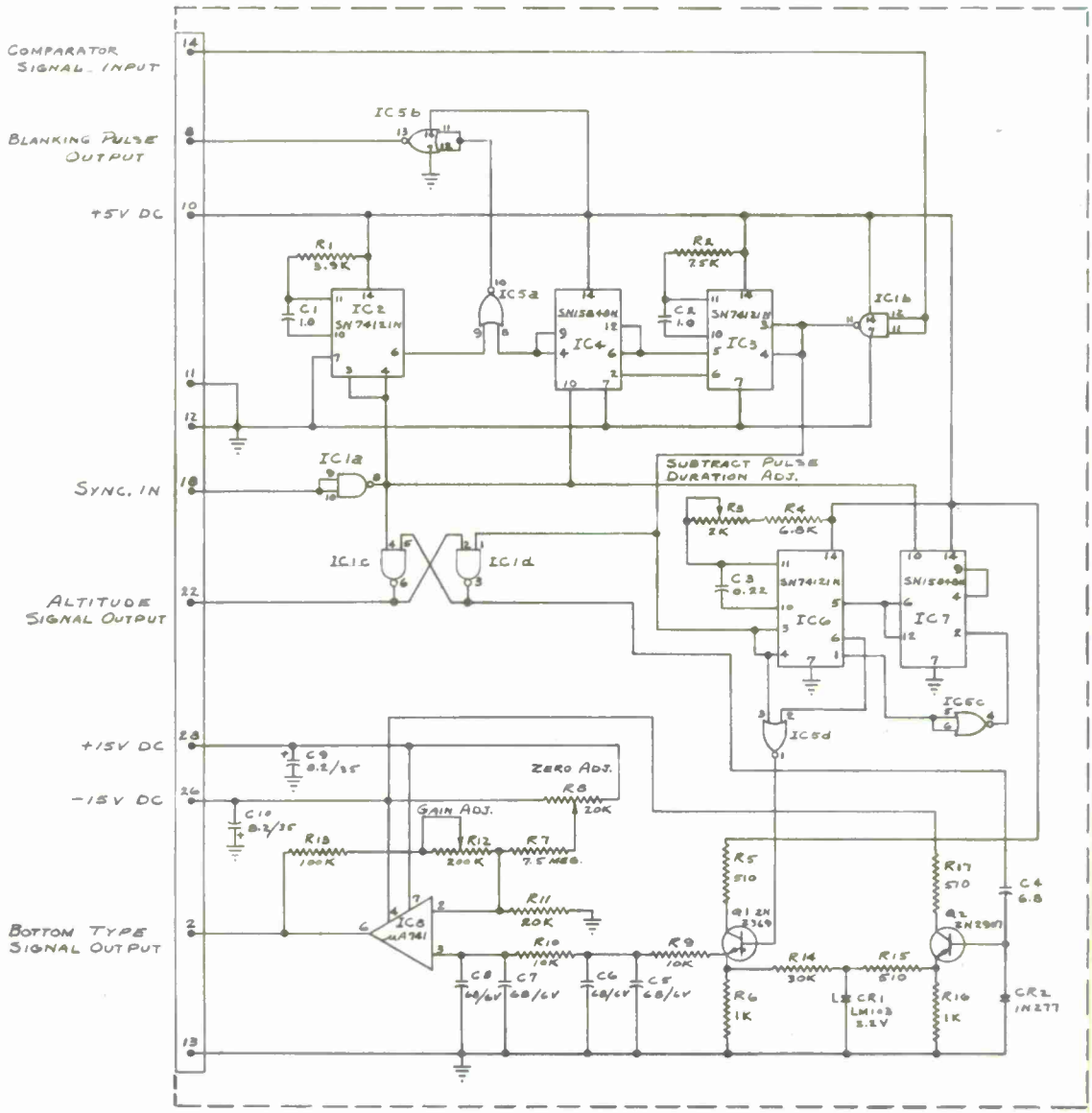


FIGURE A3. SBC LOGIC AND PROCESSING BOARD B SCHEMATIC

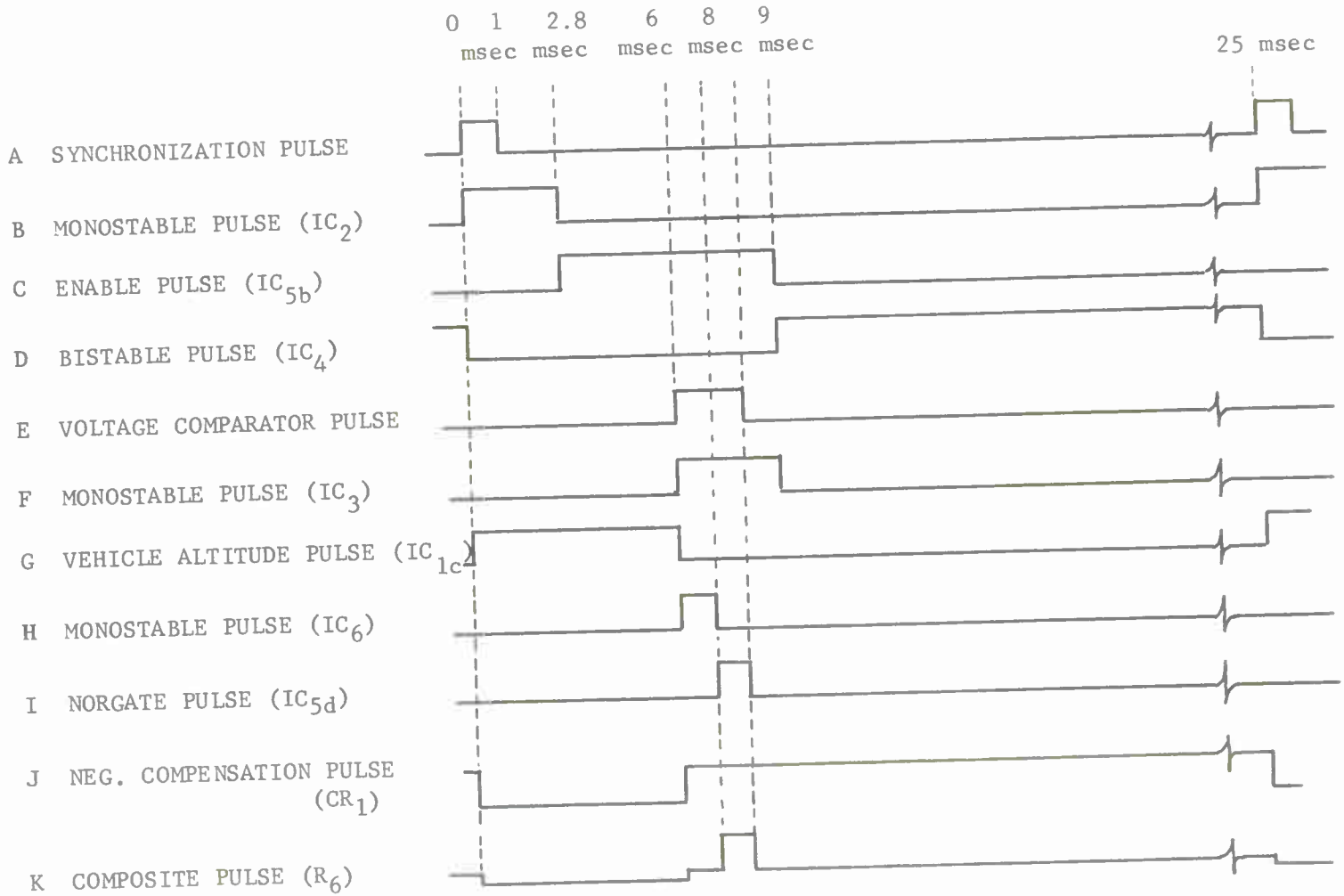


FIGURE A4. SBC LOGIC TIMING DIAGRAM

attenuated to give the proper degree of compensation and added to the bottom type difference pulse across resistor R_6 as shown in Figure A4k. The composite pulse then consists of positive and negative fixed-amplitude pulses. The time duration of the positive pulse is proportional to the bottom type while the time duration of the negative pulse is proportional to the vehicle altitude. The composite pulse is applied to the rc low-pass network consisting of resistors R_9 and R_{10}, and capacitors C_5, C_6, C_7, and C_8. The output signal of the rc network is a dc voltage, the value of which is proportional to the sum of the average value of the positive difference-pulse time duration and the average value of the negative altitude-pulse time duration. This dc voltage is amplified to a level sufficient to drive the chart recorder by integrated circuit operational amplifier IC_8.

INTERFACE BOARD D

The schematic diagram of the interface circuit board D is shown in Figure A5. Transistors Q_1 and Q_2 are operated as saturated pulse amplifiers while Q_3 is a conventional emitter follower. The vehicle-altitude-signal pulse is amplified to produce a positive pulse the maximum amplitude of which is approximately 65 volts as determined by the value of the calibration control, resistor R_6. The quiescent (no pulse) output level of Q_3 is 2.2 volts as determined by reference diode CR_3. The amplified pulse is applied to a two-section rc low-pass network consisting of resistors R_8 and R_9, and capacitors C_2 and C_3. The output signal of this network is an analog dc voltage, the amplitude of which is proportional to the towed vehicle altitude and is compatible with the vehicle-control-surface-servo system.

POWER SUPPLY BOARD E

The schematic circuit diagram of the power supply board E is shown in Figure A6. The transformer T_1 provides low ac voltage to power supply board E. Diodes CR_1, CR_2, CR_3, and CR_4 comprise two full wave rectifiers. Capacitors C_1 and C_2 smooth the pulsating dc output voltage from the rectifiers to provide positive and negative 21-volt dc voltages. The power supply regulators are integrated-circuit voltage regulators used with external series regulator transistors to provide regulated supply voltages of plus 15 volts, plus 5 volts, and minus 15 volts dc.

The SBC wiring diagram, Figure A7, shows the interconnections of the various circuit boards.

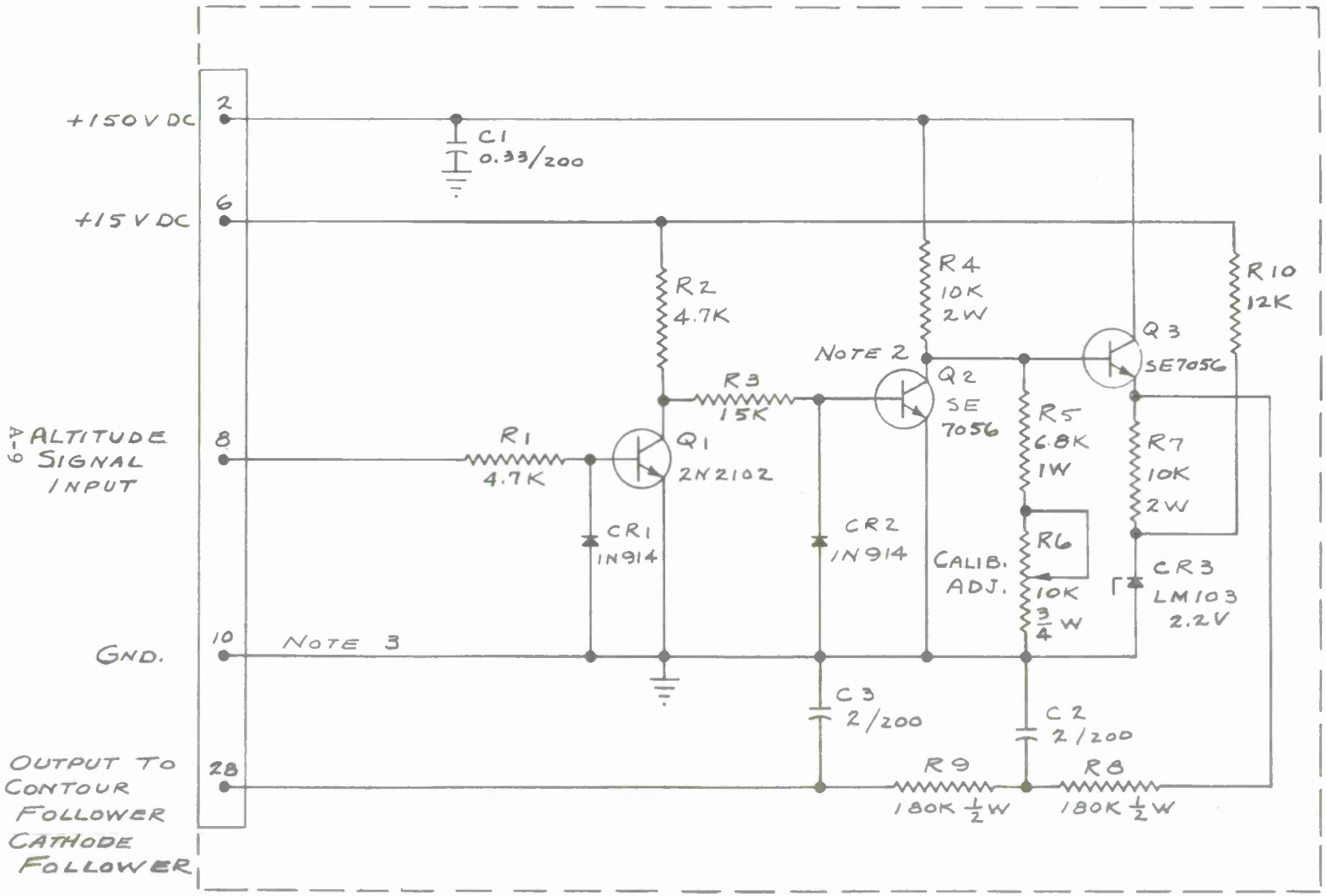


FIGURE A5. SBC INTERFACE BOARD D SCHEMATIC

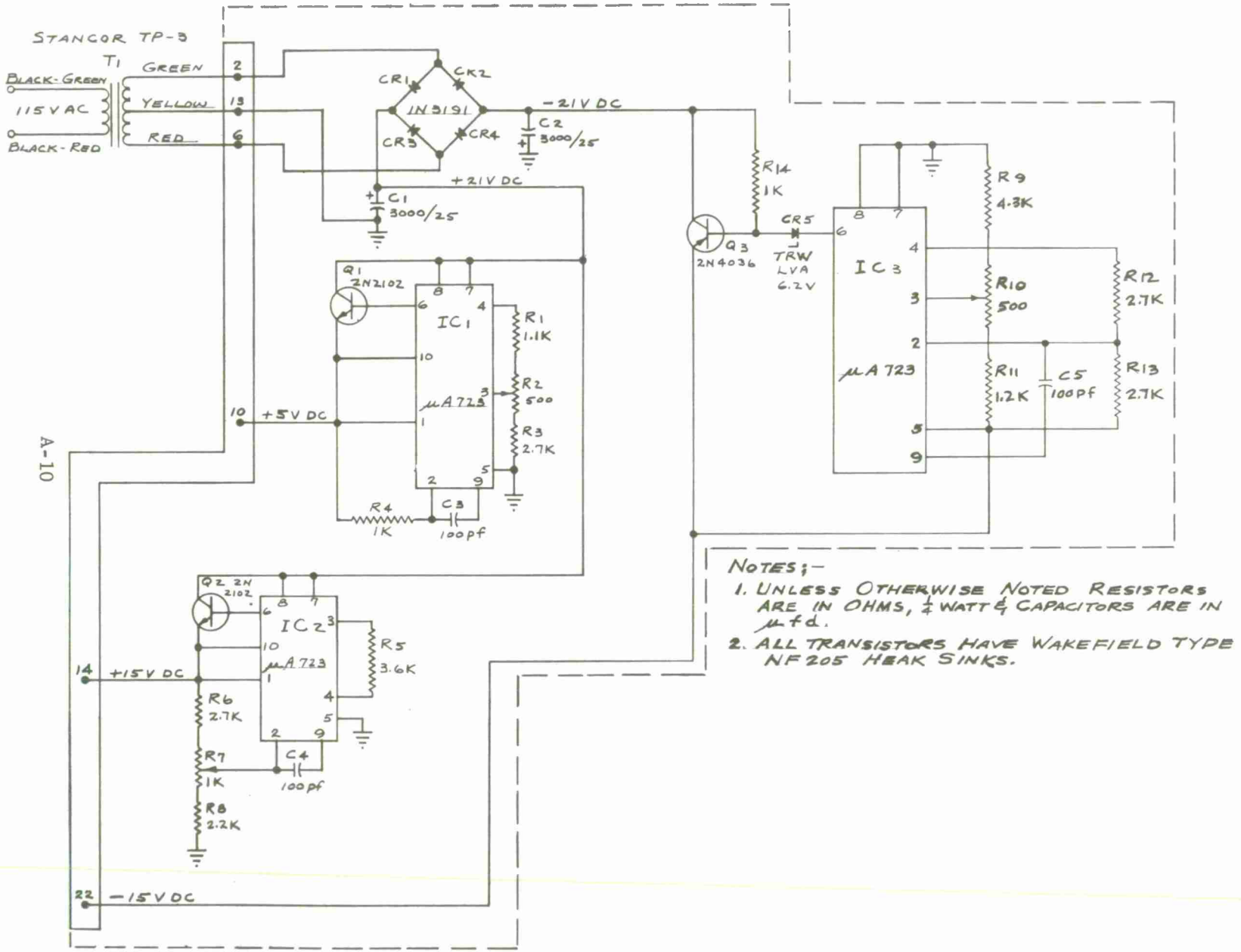


FIGURE A6. SBC POWER SUPPLY BOARD E SCHEMATIC

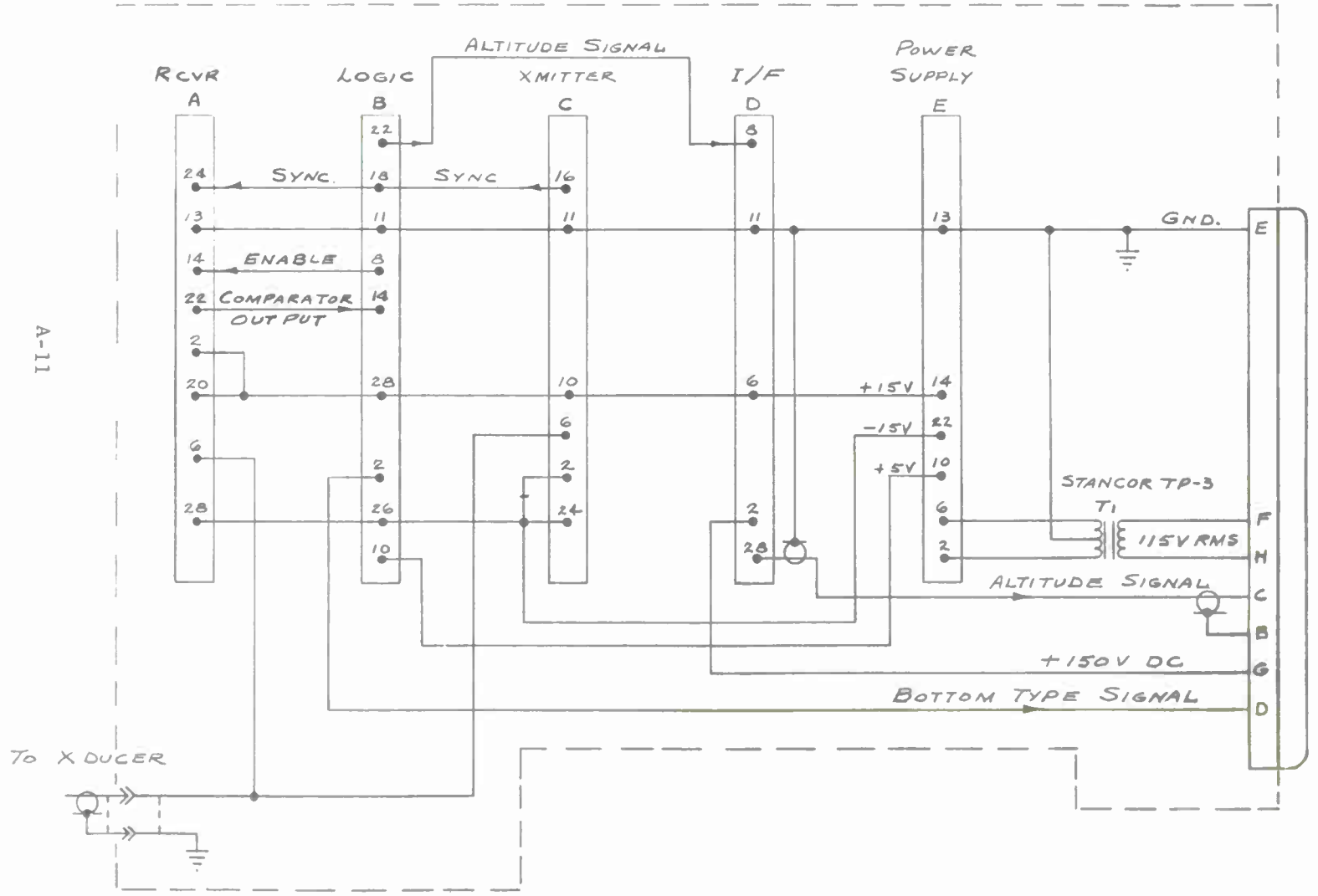


FIGURE A13. SBC WIRING DIAGRAM

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13. ABSTRACT

An improved Sea Bottom Classifier device configured for use with a towed underwater vehicle is described. Operating on the same basic principles as earlier models, but including several refinements, the device provides a relative indication of sea bottom hardness. Some preliminary sea test results are given along with a detailed discussion of the circuits of the improved device.

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